CLAIMS

What is claimed is:

1. A resistive cross point array memory device, comprising:

a plurality of word lines extending in a first direction;

a plurality of bit lines extending in a second direction such that a plurality of cross points is formed at intersections between the word and bit lines;

at least one memory element formed in at least one of the cross points, the memory element comprising a first tunnel junction, the first tunnel junction comprising a bottom conductor, a top conductor, and a barrier layer adjacent the bottom conductor; and

wherein the bottom conductor comprises a non-uniform upper surface.

2. The memory device of claim 1 wherein the bottom conductor further comprises one of the word lines and the top conductor comprises one of the bit lines.

3. The memory device of claim 1 wherein the first tunnel junction is an anti-fuse.

4. The memory device of claim 3 wherein the memory element further comprises an isolator element in series with the anti-fuse.

5. The memory device of claim 4 wherein the isolator element is selected from the group consisting of a second tunnel junction, a magnetic tunnel junction, a diode and a resistor.

6. The memory device of claim 3 wherein the average thickness of the barrier layer is between 10 and 30 angstroms.

7. The memory device of claim 3 wherein the barrier layer has a dielectric breakdown voltage of between 2 and 3 volts.

8. The memory device of claim 3 wherein the at least one memory element further comprises one of the memory elements formed at each cross point.

9. A tunnel junction for use in a memory element, comprising:

a bottom conductor comprising an upper surface;

a top conductor;

a barrier layer disposed between the bottom conductor and the top conductor; and

wherein the barrier layer comprises a non-uniform surface.

10. The tunnel junction of claim 9 wherein the tunnel junction is an anti-fuse.

11. The tunnel junction of claim 10 wherein the average thickness of the barrier layer is between 10 and 30 angstroms.

12. The tunnel junction of claim 10 wherein the barrier layer has a dielectric breakdown voltage of between 2 and 3 volts.

13. A method of producing a tunnel junction for use in a memory element, comprising:

providing a bottom conductor;

creating a non-uniform surface on the barrier layer;

depositing a barrier layer on the non-uniform upper surface; and

depositing a top conductor such that the barrier layer is disposed between the bottom conductor and the top conductor.

14. The method of claim 13 wherein the step of creating a non-uniform upper surface is accomplished using an ion etch technique.

15. A memory element comprising:

an anti-fuse comprising a bottom conductor, a top conductor, and a barrier layer of non-uniform thickness therebetween;

an isolator element in series with the first tunnel junction; and

wherein the barrier layer has a dielectric breakdown voltage of between 2 and 3 volts.

16. The memory element of claim 15 wherein the isolator element is selected from the group consisting of a second tunnel junction, a magnetic tunnel junction, a diode and a resistor.